Our Reference: 200209306-1 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants:	Theodore I. Kamins, et al.
Serial Number:	10/690,688
Filing Date:	October 21, 2003
Confirmation No.:	6130
Examiner/Group Art Unit:	Robert M. Kunemund/1722
Title:	METHOD OF FORMING THREE-DIMENSIONAL NANOCRYSTAL ARRAY

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please enter the following Appeal Brief in the appeal filed August 30, 2007.

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I. REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, L.P., a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249, Houston, Texas 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. RELATED APPEALS AND INTERFERENCES

Appellants and the undersigned attorneys are not aware of any appeals or any interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1, 5-24 and 28-40 are the claims on appeal. *See,* Appendix.

Claims 2-4 and 25-27 were cancelled.

Claims 1, 5-24 and 28-40 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Claims 1, 5-7, 10-18, 20-24 and 28-40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Li et al. (U.S. Patent No. 6,831,017, referred to hereinafter as "Li") in view of Gudiksen et al. ("Growth of nanowire superlattice structures for nanoscale photonics and electronics" Nature, Vol. 415, Feb. 7, 2002, pp. 617-620, referred to hereinafter as "Gudiksen").

Claims 8, 9 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Li in view of Gudiksen.

IV. STATUS OF AMENDMENTS

In response to the Final Office Action of May 30, 2007, no amendment pursuant to 37 C.F.R. § 1.116 was filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In this summary of claimed subject matter, all citations are to the specification of United States Patent Application serial number 10/690,688. Further, all citations are illustrative, and support for the cited element may be found elsewhere in the specification.

Independent claim 1:

A method of controllably forming a three-dimensional assembly of isolated nanowires is disclosed. Each nanowire comprises at least two materials within a matrix of another material (see paragraphs 0033 – 0035 and Figure 3c). This embodiment of the method comprises providing a substrate (see paragraphs 0027 and 0030); forming a two-dimensional catalyst array on a major surface of said substrate (see paragraphs 0026, 0028 and 0030); controllably growing in a third dimension an array of said nanowires corresponding with said catalyst array, said nanowires each comprising said at least two materials (see paragraphs 0031, 0032, 0039, 0043 and 0045, and Figures 3b and 3c); and forming the matrix of the other material that fills in spaces between said nanowires (see paragraphs 0033 – 0034 and 0043, and Figure 3c).

Independent claim 15:

A method of controllably forming a three-dimensional assembly of isolated nanowires of two materials within a matrix of one of said two materials is also disclosed.

This embodiment of the method comprises providing a substrate (see paragraphs 0027 and 0030); forming a two-dimensional catalyst array on a major surface of said substrate (see paragraphs 0026, 0028 and 0030); controllably growing in a third dimension an array of said nanowires corresponding with said catalyst array, said nanowires each comprising alternating regions of said two materials (see paragraphs 0031, 0032, 0039, 0043 and 0045, and Figures 3b and 3c); and forming a matrix of one of said materials that fills in spaces between said nanowires (see paragraphs 0033 – 0034 and 0043, and Figure 3c).

Independent claim 24:

A two-dimensional assembly of isolated nanowires or segments of nanowires is disclosed. Each nanowire comprises at least two materials within a matrix of at least one other material, wherein said isolated nanowires or segments of nanowires extend in a third dimension (see paragraphs 0031 - 0033, 0039, 0043 and 0045, and Figure 3c).

Independent claim 31:

A photonic bandgap structure is also disclosed. The photonic bandgap structure comprises an assembly of isolated nanowire segments of a first material within a matrix of a second material (see paragraphs 0028, 0033, and Figure 3c).

Independent claim 33:

A quantum dot structure is also disclosed. The quantum dot structure comprises nanowires comprising an array of controllably placed isolated segments of a first material surrounded on top and bottom by a second material and on the sides by a matrix of a third material, which may be the same as said second material or another material other than said first material, the dimensions of said isolated segments being small enough to provide quantum confinement (see paragraphs 0039 - 0041, 0043 and 0045).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1, 5-24 and 28-40 are unpatentable under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Whether claims 1, 5-7, 10-18, 20-24 and 28-40 are unpatentable under 35 U.S.C. § 103(a), as being obvious over Li in view of Gudiksen.

Whether claims 8, 9 and 19 are unpatentable under 35 U.S.C. § 103(a), as being obvious over Li in view of Gudiksen.

VII. ARGUMENTS

A. Rejection of claims 1, 5-24 and 28-40 under 35 U.S.C. § 112, first paragraph

Claims 1, 5-24 and 28-40 stand rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. According to the Examiner, there is no "teaching in the specification for controllably forming in 3d as is now claimed and no support for growth in the 3d."

Appellants strongly disagree with the Examiner. It is submitted that controllable growth in the third-dimension is taught throughout the specification as filed, at least at paragraphs 0013, 0039 and 0041, and in Figures 1c, 2, and 3a through 3c. In particular, the controlled nanowire growth includes positioning the particles on the major surface of the substrate (as described in paragraphs 0022-0025), positioning the particles so there is sufficient epitaxial contact between the catalyst and the substrate (as shown in Fig. 2), positioning particles of a uniform size (as shown in Fig. 1c), and exposing the particles to two or more gases (as described in paragraph 0029).

Furthermore, it is submitted that controllable growth in the third-dimension is taught at least in the following non-limiting examples:

1) paragraph 0039 states in part:

> Thus, small catalyst nanoparticles (leading to narrow diameter nanowires) and short isolated segments can create quantum dots. Thus, the isolated segments are **controllably placed in all three dimensions**. (emphasis added)

2) paragraphs 0030 – 0031 state in part:

> As shown in FIG. 3a, a catalyst array 114 [*shown in two dimensions*], comprising a plurality of catalyst nanoparticles 14, is formed on a surface 16a [*shown as a two dimensional surface*] of substrate 16, ...
>
> In FIG. 3b, an array 118 of nanowires 18 [*shown in the third dimension*] is next formed, again employing the techniques described above [*for example, with regard to Fig. 2, which shows growth of nanowire 18 into the third dimension from the two dimensional substrate surface 16a*]. (explanation added)

3) paragraph 0043 states in part:

> The segments 18a, 18b are **grown** by simply **controlling** the gas flow of one or the other of the foregoing gaseous compounds. (emphasis added)

4) paragraph 0045 states in part:

> The nanowire growth can be terminated by removing the catalyzing nanoparticle [*particle 14 is shown at the tip of nanowire 18 in Fig. 3b*] at the tip of the wire; . . . . Alternatively, the deposition conditions can be changed so that catalytic growth is no longer favored over normal growth. (explanation added)

The Examiner further states in his "Response to Applicants' Arguments" that "[t]here is no teaching in the specification which even alludes to the control as is now set forth." In sharp contrast to the Examiner's assertion, it is clear, at least from the above citations, quotes and the figures referred to therein (as well as Appellants' application as a

whole), that there is clear support for controllably forming in 3D and growth in 3D. As such, it is submitted that the Examiner's assertion is clearly erroneous.

Further regarding the written description requirement, the courts have held that the subject matter of the later claim need not be described literally or "*in ipsis verbis*" in order for the specification to satisfy the description requirement. See, e.g., *Cordis Corp. v. Medtronic AVE, Inc.*, 339 F.3d 1352 (Fed. Cir.), reh'g denied, 2003 U.S. App. LEXIS 22508 (2003); and *In re Lukach*, 442 F.2d 967, 969, 169 U.S.P.Q. 795, 796 (C.C.P.A. 1971).

For all the reasons provided hereinabove, it is submitted that the support for the recitation of controllably forming or growing nanowires in the third dimension may, indeed, be gleaned from the specification and drawings as originally filed and as understood in their totality. As such, it is submitted that the rejection under 35 U.S.C. § 112, first paragraph is erroneously based, and withdrawal of the same is respectfully requested.

B. Rejection of claims 1, 5-7, 10-18, 20-24 and 28-40 under 35 U.S.C. § 103(a)

Claims 1, 5-7, 10-18, 20-24 and 28-40 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Li in view of Gudiksen. The Examiner states that Li fails to teach that the nanowires are made of two different materials. The Examiner then states that Gudiksen teaches growing nanowires having two different materials. The Examiner concludes that it would have been obvious to the skilled artisan to modify Li to have two materials in the nanowire in order to create diverse applications for the nanowire structure.

a. Claims 1, 5, 6, 10-18, 20-24, 28, 29, 38 and 39

Appellants are controllably growing two-material nanowires from a two dimensional surface into a third dimension. Li teaches growing single material nanowires. Gudiksen teaches growing two-material nanowires on a two dimensional surface (it does not appear that the nanowires are attached to the substrate surface), and then removing the nanowires for desired applications.

The Examiner has not provided a suggestion gleaned from either of the references as to why a skilled artisan would assume that methods for growing nanowires in two dimensions, apparently not attached to a substrate surface (Gudiksen) would be appropriate for incorporating into a method for growing nanowires that remain on a substrate surface (Li). In fact, Appellants submit that the skilled artisan would not be so led to combine Li and Gudiksen in the manner suggested by the Examiner, at least for the reasons set forth below and in the previously filed Declaration pursuant to 37 C.F.R. § 1.132 (submitted herein as evidence).

In the Office Action dated November 14, 2006, the Examiner stated that the Li reference is clearly broader than what is set forth in Appellants' 132 Declaration. The Examiner concluded that "[t]he Li et al reference does not require an electric field and discloses other methods of array nanowire growth. Electric fields are taught to align or orientate only."

Li does suggest that any suitable technique, such as thermal and plasma chemical vapor deposition, may be used to grow nanowires. Li also states that the substrate may be silicon, other semiconductors, quartz, sapphire, and glass. However, Li does not teach or suggest that any of these substrates is a single-crystal substrate with the proper orientation (e.g., (111)) for growing vertical nanowires. Appellants submit that without a single-crystal substrate, the nanowires of Li are not likely to grow vertically without the additional exposure to an electric field (which vertically orients the nanowires of Li, see Col. 5, lines 25-32).

Furthermore, Li illustrates (in Figures 1a, 1b, 2a-2e, 3a-3c, 4a-4d, 5a-5c and 7) that vertical nanowires are formed on an electrode pad that is formed on the surface of the substrate prior to nanowire growth (see also, Col. 4, lines 9-19). However, Appellants submit that the electrode pad of Li is NOT a single-crystal substrate, and as such, it is unlikely that such nanowires will be vertical without some additional orientation process (such as that described by Li) or unless all of the grains in the underlying metal electrode are properly oriented, the latter of which is not likely.

Therefore, while Li does suggest that any suitable technique, such as thermal and plasma chemical vapor deposition techniques, may be used to grow nanowires, Li does

NOT teach or suggest other methods (aside from exposure to an electric field) to vertically orient and enhance the uniformity (e.g., verticality) of the grown nanowires. As such, it is submitted that the scope of Li is rather limited in the description of forming a **vertically oriented** assembly of nanowires.

In this regard, Appellants submit that the previously filed 132 Declaration supports the contention that Li and Gudiksen would not be combined by one skilled in the art. Li specifically states that vertical growth may be controlled by exposing the nanowires to an electric field (external or from plasma). One skilled in the art would conclude from this teaching that the nanowire diameter of Li must be thin enough to be manipulated by the applied electric field taught by Li (about 700 V/cm), as this is the only method of alignment taught by Li.

It is submitted that the nanowires of Gudiksen have a thickness that would require an external electric field for alignment much larger than the 700 V/cm taught by Li (for example, as stated in the previously filed 132 Declaration, a field of about $E > 10^6$ V/cm would be required to align a nanowire having a diameter of 20 nm). The field intensity required to align a nanowire having a 20 nm diameter is significantly larger (greater than 1400 times larger) than the 700 V/cm taught by Li. Further, in addition to this very large field, it is submitted that undue experimentation and extensive procedures of the process (which procedures are not taught in either of Li or Gudiksen) would be required to successfully align the nanowires in this manner. In addition to these procedures not being taught or suggested (or even within the skill set of the ordinarily skilled artisan), such procedures would be so complicated as to render the Examiner's suggested combined process impractical for use (see 132 Declaration for further discussion).

Furthermore, it is submitted that if one skilled in the art were to attempt to use the plasma taught in Li to align the segmented nanowires taught in Gudiksen, one would likely damage at least one segment of the Gudiksen nanowires for reasons discussed in the 132 Declaration. Further, it is submitted that the net or DC field provided by the plasma is too low to achieve a sufficiently high aligning electric field.

The Examiner does point out that Li suggests that the nanowire diameter may be larger (from 5 nm to 200 nm, see Col. 4, lines 59-63). However, taking into consideration

the electric field taught by Li (i.e., 700 V/cm) used to vertically orient nanowires and the evidence set forth in the 132 Declaration, it is submitted that the suggested nanowire diameter of Li is inconsistent with the vertical orientation method taught in Li. As such, in view of this teaching and the submitted evidence, it is further submitted that one skilled in the art still would not combine Li with Gudiksen.

For all the foregoing reasons, Appellants submit that Li does not teach the formation of vertical nanowires without the additional exposure to an electric field, and if one skilled in the art were to use the electric field of Li with the nanowires of Gudiksen, such procedures would be so complicated as to render the Examiner's suggested combined process impractical for use and would likely damage at least one segment of the Gudiksen nanowires.

Still further, the Appellants respectfully submit that Gudiksen does not teach or suggest any reason for removal of the **native oxide** from the substrate upon which the nanowires are grown. It is submitted that vertical nanowires cannot be grown from such a substrate having the native oxide thereon. As Gudiksen teaches removal of the nanowires from the substrate after growth, the alignment of the nanowires during growth is not important. The random direction that one can achieve on an amorphous surface, such as a native oxide, is adequate if one is planning to remove nanowires from the substrate after growth. Therefore, one would not be led by Gudiksen to remove the native oxide layer to form vertical nanowires. As such, if one applied the Gudiksen methods to the Li methods, vertical nanowires would fail to grow, thus *destroying the stated purpose* of the Li reference.

For all of these reasons, Appellants submit that their invention as defined in independent claims 1, 15 and 24, and in those claims depending ultimately therefrom, is not anticipated, taught or rendered obvious by the cited references, either alone or in combination, and patentably defines over the art of record.

b. Claims 7 and 30

The Examiner stated in his "Response to Applicants' Arguments" that the "Li et al reference does not limit the matrix to one particular type." He goes on to state that "It does mention amorphous but is not limited in scope and thus reads on the claims."

At the outset, Appellants reiterate the arguments set forth hereinabove regarding independent claims 1 and 24, from which claims 7 and 30, respectively, depend. For at least these reasons, Appellants submit that claims 7 and 30 are patentable because of their respective dependency from claims 1 and 24.

Furthermore, Appellants recite materials that form **crystalline nanowires in a matrix of a crystalline material**. In sharp contrast, Li teaches *amorphous matrix materials*, and Gudiksen teaches crystalline nanowires, but *no matrix*.

As previously stated, the Examiner concludes that Li is not limited to amorphous matrix materials. Contrary to the Examiner's conclusion, however, Li does **not** teach or suggest any suitable alternatives for the amorphous materials listed (see Col. 6, lines 21-49), and Gudiksen does not supply this deficiency.

Still further, Appellants respectfully submit that the three-dimensional nanocrystal array of Appellants' invention as defined in claims 7 and 30 cannot be achieved in an amorphous matrix. In one non-limiting example, in order to obtain isolated nanocrystals embedded in a uniform matrix, the matrix is the same material and has the same crystal structure as the segments surrounding the segment that becomes the isolated nanocrystal. Therefore, an amorphous matrix (as taught by Li) does not satisfy the components for this structure (i.e., crystalline nanowires in a matrix of a crystalline material), and thus would not render obvious Appellants' invention as recited in claims 7 and 30.

For all these reasons, Appellants submit that their invention as defined in claims 7 and 30 is not anticipated, taught or rendered obvious by the cited references, either alone or in combination, and patentably defines over the art of record.

c. Claims 31, 32 and 40

At the outset, Appellants reiterate the arguments set forth hereinabove regarding independent claims 1, 15 and 24. For at least these reasons, Appellants submit that claims 31, 32 and 40 are patentable.

Furthermore, Appellants submit that neither Li nor Gudiksen teach or suggest a photonic bandgap structure. It is further submitted that such a structure would not be obvious in view of the teachings of these references. For all these reasons, Appellants submit that their invention as defined in claims 31, 32 and 40 is not anticipated, taught or rendered obvious by the cited references, either alone or in combination, and patentably defines over the art of record.

d. Claims 33- 37

At the outset, Appellants reiterate the arguments set forth hereinabove regarding independent claims 1, 15 and 24. For at least these reasons, Appellants submit that claims 33 through 37 are patentable.

Furthermore, Appellants submit that neither Li nor Gudiksen teach or suggest a quantum dot structure. It is further submitted that such a structure would not be obvious in view of the teachings of these references. For all these reasons, Appellants submit that their invention as defined in claims 33 through 37 is not anticipated, taught or rendered obvious by the cited references, either alone or in combination, and patentably defines over the art of record.

C. Rejection of claims 8, 9 and 19 under 35 U.S.C. § 103(a)

Claims 8, 9 and 19 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Li in view of Gudiksen. The Examiner **admits** that neither of the references teaches a mold for applying the catalyst material, as recited by the Appellants. The Examiner concludes however, that in the absence of unexpected results, it would have been obvious to one of ordinary skill in the art through routine experimentation to find the optimum, operable means to pattern and apply the catalyst of Li.

Obviousness is a question of law based on (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness. *Graham v. John Deere Co.*, 383, U.S. 1, 17, 148 USPQ 459, 467 (1966). An invention may be obvious if it merely combines "familiar elements according to known methods [to] yield predictable results." *KSR Int. Co. v. Teleflex Inc. et al.*,127 S.Ct. 1727; 167 L.Ed. 2d 705; 2007 U.S. LEXIS 4745; 75 U.S.L.W. 4289; 82 U.S.P.Q.2d (BNA) 1385 (2007).

A basic requirement to establish a case that a claim is *prima facie* obvious is that "the prior art reference (or references when combined) must teach or suggest all the claim limitations" M.P.E.P. §2143. "In proceedings before the Patent and Trademark Office, the Examiner bears the burden of establishing a *prima facie* case of obviousness based upon the prior art." *In re Fritch*, 972 F.2d 1260, 1265, 23 USPS2d 1780, 1783 (Fed. Cir. 1992). "If examination at the initial stage does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of the patent." *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

a. <u>Claims 8 and 19</u>

At the outset, Appellants reiterate the arguments set forth hereinabove regarding independent claims 1 and 15, from which claims 8 and 19 respectively depend. For at least these reasons, Appellants submit that claims 8 and 19 are patentable because of their respective dependency from claims 1 and 15.

Li teaches a template that is capable of absorbing catalyst in solution (i.e., catalyst ink). This template may be used to transfer the absorbed catalyst onto a substrate surface (see Col. 8, lines 52-57). It is submitted that Li's teaching regarding the template is extremely limited, in part because the template is only described as being capable of absorbing catalyst ink. Li specifically explains that the template is formed of a material (e.g., a polymer) that can be impregnated or soaked with the catalyst solution (see Col. 8, line 58 through Col. 9, line 19 and claim 9).

The teachings of Li are in sharp contrast to the mold used in Appellants' claims 8 and 19. The specification as filed, at paragraphs 0024 and 0025, states that the mold

(of claims 8 and 19) is formed of a relatively hard material that is coated with a material containing the desired catalyst. Appellants' mold is not capable of absorbing catalyst in solution, as the mold "can be made of materials such as metals, dielectrics, semiconductors, ceramics, or their combination." (See paragraph 0025 of Appellants' specification as filed). These materials will not absorb a catalyst in solution. In fact, the Appellants' mold, as recited in claims 8 and 19, is coated with a material containing the catalyst.

Furthermore, it is submitted that a template suitable for soaking up a catalyst solution (Li) does not anticipate or render obvious a mold suitable for receiving a coating of a catalyst containing material. The characteristics of the template of Li contradict the characteristics of the Appellants' mold, and it is submitted that the stated purpose of the template of Li (to transfer a catalyst **solution**) would be destroyed if the template could not absorb. As such, Appellants submit that coating a mold (as recited in claims 8 and 19) is not an obvious variation of or replacement for absorbing the catalyst solution of Li.

As such, Appellants respectfully submit that the Examiner has failed to set forth a *prima facie* case of obviousness regarding claims 8 and 19. As neither of the cited references teaches or suggests the specific method steps recited in claims 8 and 19, it is submitted that the Examiner has failed to establish a *prima facie* case of obviousness.

For all these reasons, Appellants submit that their invention as defined in claims 8 and 19 is not anticipated, taught or rendered obvious by the cited references, either alone or in combination, and patentably defines over the art of record.

b. Claim 9

At the outset, Appellants reiterate the arguments set forth hereinabove regarding independent claim 1, from which claim 9 depends. For at least these reasons, Appellants submit that claim 9 is patentable because of its dependency from claim 1.

Appellants further respectfully submit that the Examiner has failed to set forth a *prima facie* case of obviousness regarding claim 9. Neither of the cited references teaches or suggests any of these steps:

imprinting a first line of material over a layer of said catalyst material;

etching to remove catalyst material where not protected;

imprinting a second line of material orthogonal to said first line; and

etching to remove catalyst material where not protected, so that said catalyst only remains where protected by both imprints.

In particular, neither Li nor Gudiksen teaches or suggests imprinting a second line of material orthogonal to the first line of material. Further, as mentioned above, contrary to the Examiner's assertion, it is submitted that such steps are the result of more than routine experimentation to find the optimum, operable means to pattern and apply the catalyst of Li, especially in view of the fact that Li specifically teaches methods for forming catalyst sites, including lithography, metal migration, metal evaporation, lift-off, etc. **without mentioning molding in two steps resulting in lines orthogonal to each other** (see Col. 1, lines 50-67).

For all these reasons, Appellants submit that their invention as defined in claim 9 is not anticipated, taught or rendered obvious by the cited references, either alone or in combination, and patentably defines over the art of record.

SUMMARY

The Appellants respectfully submit that claims 1, 5-24 and 28-40 herein fully satisfy the requirements of 35 U.S.C. §§ 112, 102 and 103. In view of the foregoing, favorable consideration and passage to issue of the present application is respectfully requested. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

1. (Previously presented) A method of controllably forming a three-dimensional assembly of isolated nanowires, each nanowire comprising at least two materials within a matrix of an other material, said method comprising:

providing a substrate;

forming a two-dimensional catalyst array on a major surface of said substrate;

controllably growing in a third dimension an array of said nanowires corresponding with said catalyst array, said nanowires each comprising said at least two materials; and

forming the matrix of the other material that fills in spaces between said nanowires.

2 - 4. (Canceled)

5. (Previously presented) The method of Claim 1 wherein said isolated nanowires of the at least two materials comprise alternating regions of a first material and a second material, and wherein said matrix comprises a third material.

6. (Original) The method of Claim 5 wherein said first material is selected from the group consisting of silicon, germanium, GaAs, GaP, InAs, InP, mixed III-V compound semiconductor materials, CdS, CdTe, and mixed II-VI compound semiconductor materials, wherein said second material is selected from the group consisting of silicon, germanium, GaAs, GaP, InAs, InP, mixed III-V compound semiconductor materials,

CdS, CdTe, and mixed II-VI compound semiconductor materials, and wherein said first material is different than said second material.

7. (Original) The method of Claim 6 wherein said third material is selected from the group consisting of silicon, germanium, GaAs, GaP, InAs, InP, mixed III-V compound semiconductor materials, CdS, CdTe, mixed II-VI compound semiconductor materials, oxides, nitrides, and oxynitrides, and wherein said third material may be the same or different than either said first material or said second material.

8. (Original) The method of Claim 1 wherein said step of forming said catalyst array comprises:

providing a mold with nanoscale protrusions forming all the individual elements of a desired pattern;

coating said protrusions with a material containing said catalyst;

providing a substrate; and

transferring said catalyst to a major surface of said substrate, said major surface comprising a non-catalytic surface, to form a pattern of said catalyst on said major surface of said substrate.

9. (Original) The method of Claim 1 wherein said step of forming said catalyst array comprises:

imprinting a first line of material over a layer of said catalyst material;

etching to remove catalyst material where not protected;

imprinting a second line of material orthogonal to said first line; and

etching to remove catalyst material where not protected, so that said catalyst only remains where protected by both imprints.

10. (Previously presented) The method of Claim 1 wherein said step of growing said array of nanowires comprises:

introducing a gaseous source containing at least one of the at least two materials; and

allowing said gaseous source to react with said catalyst and diffuse therethrough or therearound, thereby causing precipitation of said at least one of the at least two materials, thereby forming said nanowires.

11. (Original) The method of Claim 10 wherein two materials are used to form said nanowires having alternating regions of a first material and a second material by:

introducing a first gaseous source containing said first material;

allowing said first gaseous source to react with said catalyst and diffuse therethrough, thereby causing precipitation of said first material, thereby forming one segment;

introducing a second gaseous source containing said second material;

allowing said second gaseous source to react with said catalyst and diffuse therethrough, thereby causing precipitation of said second material, thereby forming a second segment; and

alternating said first gaseous source and said second gaseous source to thereby form said nanowire comprising said alternating regions.

12. (Original) The method of Claim 11 wherein one of said gaseous sources comprises silane and said material precipitated is silicon and wherein another of said gaseous sources comprises germane and said material precipitated is germanium.

13. (Original) The method of Claim 1 wherein said step of forming said matrix comprises a non-catalytic method.

14. (Original) The method of Claim 13 wherein said matrix is formed by chemical vapor deposition or by directional filling using physical vapor deposition or by high-density plasma-enhanced chemical vapor deposition.

15. (Previously presented) A method of controllably forming a three-dimensional assembly of isolated nanowires of two materials within a matrix of one of said two materials, said method comprising:

providing a substrate;

forming a two-dimensional catalyst array on a major surface of said substrate;

controllably growing in a third dimension an array of said nanowires corresponding with said catalyst array, said nanowires each comprising alternating regions of said two materials; and

forming a matrix of one of said materials that fills in spaces between said nanowires.

16. (Original) The method of Claim 15 wherein said substrate comprises silicon, said nanowires comprise alternating regions of germanium and silicon, and said matrix comprises silicon.

17. (Original) The method of Claim 15 wherein said catalyst array comprises a metal that catalyzes growth of said nanowires from vapors comprising precursors of said two materials.

18. (Original) The method of Claim 17 wherein said metal comprises gold and wherein said vapors comprise germane and silane, alternately introduced to be catalyzed by said gold to form said alternating regions of germanium and silicon.

19. (Previously presented) The method of Claim 15 wherein said step of forming said catalyst array comprises:

providing a mold with nanoscale protrusions forming all the individual elements of a desired pattern;

coating said protrusions with a material containing said catalyst;

providing a substrate; and

transferring said catalyst to a major surface of said substrate, said major surface comprising a non-catalytic surface, to form a pattern of said catalyst on said major surface of said substrate.

20. (Previously presented) The method of Claim 15 wherein said step of growing said array of nanowires comprises:

introducing a first gaseous source containing a first material;

allowing said first gaseous source to react with said catalyst and diffuse therethrough, thereby causing precipitation of said first material, thereby forming one segment;

introducing a second gaseous source containing a second material;

allowing said second gaseous source to react with said catalyst and diffuse therethrough, thereby causing precipitation of said second material, thereby forming a second segment; and

alternating said first gaseous source and said second gaseous source to thereby form said nanowire comprising said alternating regions.

21. (Original) The method of Claim 20 wherein one of said gaseous sources comprises silane and said material precipitated is silicon and wherein another of said gaseous sources comprises germane and said material precipitated is germanium.

22. (Original) The method of Claim 15 wherein said step of forming said matrix comprises a non-catalytic method.

23. (Original) The method of Claim 22 wherein said matrix is formed by chemical vapor deposition or by directional filling using physical vapor deposition or by high-density plasma-enhanced chemical vapor deposition.

24. (Previously presented) A two-dimensional assembly of isolated nanowires or segments of nanowires, each nanowire comprising at least two materials within a matrix of at least one other material, said isolated nanowires or segments of nanowires extending in a third dimension.

25 - 27. (Canceled)

28. (Original) The assembly of Claim 24 wherein said isolated nanowires of two materials comprise alternating regions of a first material and a second material and wherein said matrix comprises a third material.

29. (Original) The assembly of Claim 28 wherein said first material is selected from the group consisting of silicon, germanium, GaAs, GaP, InAs, InP, mixed III-V compound semiconductor materials, CdS, CdTe, and mixed II-VI compound semicon-

ductor materials, wherein said second material is selected from the group consisting of silicon, germanium, GaAs, GaP, InAs, InP, mixed III-V compound semiconductor materials, CdS, CdTe, and mixed II-VI compound semiconductor materials, and wherein said first material is different than said second material.

30. (Original) The assembly of Claim 29 wherein said third material is selected from the group consisting of silicon, germanium, GaAs, GaP, InAs, InP, mixed III-V compound semiconductor materials, CdS, CdTe, and mixed II-VI compound semiconductor materials, oxides, nitrides, and oxynitrides, and wherein said third material may be the same or different than either said first material or said second material.

31. (Previously presented) A photonic bandgap structure comprising an assembly of isolated nanowire segments of a first material within a matrix of a second material.

32. (Original) The photonic bandgap structure of Claim 31 wherein said first material is selected from the group consisting of silicon, germanium, GaAs, GaP, InAs, InP, mixed III-V compound semiconductor materials, CdS, CdTe, and mixed II-VI compound semiconductor materials, wherein said second material is selected from the group consisting of silicon, germanium, GaAs, GaP, InAs, In P, mixed III-V compound semiconductor materials, CdS, CdTe, mixed II-VI compound semiconductor materials, oxides, nitrides, and oxynitrides, and wherein said said first material is different than said second material.

33. (Original) A quantum dot structure comprising nanowires comprising an array of controllably placed isolated segments of a first material surrounded on top and bottom by a second material and on the sides by a matrix of a third material, which may be the same as said second material or another material other than said first material, the dimensions of said isolated segments being small enough to provide quantum confinement.

34. (Original) The quantum dot structure of Claim 33 wherein said first material and said second material are each independently selected from the group consisting of silicon, germanium, GaAs, GaP, InAs, InP, mixed III-V compound semiconductor materials, CdS, CdTe, and mixed II-VI compound semiconductor materials.

35. (Original) The quantum dot structure of Claim 34 wherein said third material is selected from the group consisting of silicon, germanium, GaAs, GaP, InAs, InP, mixed III-V compound semiconductor materials, CdS, CdTe, mixed II-VI compound semiconductor materials, oxides, nitrides, and oxynitrides, and wherein said third material is different than said first material and may be the same or different than said second material.

36. (Original) The quantum dot structure of Claim 35 wherein said first material comprises germanium and wherein said dimensions are of the order of 10 nm.

37. (Original) The quantum dot structure of Claim 33 wherein said isolated segments are controllably placed in all three dimensions.

38. (Previously presented) The method of Claim 1 wherein two or more layers of said matrix are formed.

39. (Previously presented) The assembly of Claim 24 wherein said matrix comprises two or more layers of materials.

40. (Previously presented) The photonic band gap structure of Claim 31 comprising a plurality of nanowires, each nanowire comprising two materials within a matrix of said second material, said isolated segments of nanowires extending in a third dimension, wherein one of said materials comprises said first material and wherein another of said materials comprises the same material as said second material, thereby providing said assembly of said isolated segments of said first material.

IX. EVIDENCE APPENDIX

A copy of the Declaration pursuant to 37 C.F.R. § 1.132 filed by the Appellants on August 25, 2006 is appended hereto.

A copy of A. Ural, et al., Applied Physics Letters, vol. 81, p. 3466 (28 October 2002), filed by the Appellants as "Exhibit 1" accompanying the previously mentioned 132 Declaration is appended hereto.

A copy of H. Kam, et al., 2005 International Electron Devices Meeting, Washington DC, December 5-7, 2005, paper 19.2, filed by the Appellants as "Exhibit 2" accompanying the previously mentioned 132 Declaration is appended hereto.

X. RELATED PROCEEDINGS APPENDIX

None.

Our Reference: 200209306-1 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Theodore I. Kamins et al.
Serial Number:	10/690,688
Filing Date:	October 21, 2003
Confirmation No.:	6130
Examiner/Group Art Unit:	Robert M. Kunemund/1722
Title:	METHOD OF FORMING THREE-DIMENSIONAL NANOCRYSTAL ARRAY

DECLARATION PURSUANT TO 37 C.F.R. § 1.132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Theodore I. Kamins, hereby declare the following:

1. I am one of the inventors of the above-identified application.

2. I am a citizen of the United States, residing in Palo Alto, California.

3. I received a B.S. in Electrical Engineering from the University of California, Berkeley, located in Berkeley, CA, in 1963.

4. I received an M.S. in Electrical Engineering (Solid-State Electronics) from the University of California, Berkeley, located in Berkeley, CA, in 1965.

5. I received a Ph.D. in Electrical Engineering (Solid-State Electronics) from the University of California, Berkeley, located in Berkeley, CA, in 1968.

6. From 1968 to 1969, I was Acting Assistant Professor, Dept. of Electrical Engineering, University of California, Berkeley.

7. From 1969 to 1974, I worked at the Research and Development Laboratory of Fairchild Semiconductor, located in Palo Alto, CA.

8. In 1974, I joined Hewlett-Packard Laboratories ("HP Labs") in Palo Alto, California as a Member of the Technical Staff. I am currently a Principal Scientist in the Quantum Science Research group at HP Labs, where I am focusing on advanced nanostructured electronic materials and devices.

9. From 1999 to the present, I have been a Consulting Professor in the Electrical Engineering Department at Stanford University, located in Stanford, CA.

10. Throughout my career, I have investigated several topics, including materials and device-related areas (e.g., the development of UV-sensitive photodiodes); silicon-on-insulator and rapid thermal processing; advanced epitaxy and device technology for the silicon-germanium, heterojunction bipolar transistor; self-assembled nanostructures formed by lattice-mismatched epitaxial deposition and self-assembled nanowires grown by catalytically enhanced chemical vapor deposition.

11. After reviewing U.S. Patent No. 6,831,017, I submit that the '017 patent teaches the use of thermal and plasma chemical vapor deposition techniques (see Col. 5, lines 10-12) for nanowire growth.

12. The '017 patent states that "During plasma CVD growth, the inherent electric field produced by the plasma may help to vertically orient the nanowires 18 that are grown. An external electric field may also be applied to a plasma or thermal CVD growth chamber to enhance the uniformity (e.g., the verticality) of the nanowire alignment. A typical electric field strength that may be used to enhance nanowire alignment may be on the order of 700 V/cm." This statement indicates that the nanowires of Li must be thin enough to bend under the influence of the applied electric field, whether it is an external electric field or is provided by the plasma.

13. It is my understanding that an electric field strength of 700 V/cm is capable of aligning nanowires having diameters less than about 2 nm. (See paragraphs 15 et seq. below for a more detailed, related discussion.)

14. The '017 patent also teaches that an amorphous material (e.g., silicon oxide, polymers, spin-on-glass, see Col. 6, lines 21-49) may be used as a matrix surrounding the nanowires, contrary to the materials taught in our currently pending claims 7 and 30. I submit that a three-dimensional array of nanocrystals substantially totally surrounded by a second material is not achievable if an amorphous material is used as a matrix around crystalline nanowires. In the '017 patent, the nanowires are uniformly composed of a crystalline material, while the filling matrix material is amorphous and, therefore, different than the nanowire material.

15. I reviewed the paper by Gudiksen et al., entitled "Growth of nanowire supperlattice structures for nanoscale photonics and electronics", published in February 2002 in Nature Vol. 415, pages 617-620 (referred to herein as "the Nature Paper"). The Nature Paper teaches nanowires having about 20 nm diameters. The deflection of the nanowire in an electric field decreases as the inverse fourth power of the diameter. Field alignment works with a carbon nanotube having a diameter of about 1.4 nm. See, for example, A. Ural, et al., Applied Physics Letters, vol. 81, p. 3466 (28 October 2002) (a copy of which is attached hereto as Exhibit 1), where an electric field of ~1V/μm (10^4 V/cm) is cited as the electric field needed for alignment of CNTs. However, for a given material, when the diameter increases from 1.4 nm to 20 nm, the deflection decreases by a factor of 41,600. This decrease is partially offset to a factor of about 6000 by the higher value of Young's modulus for carbon nanotubes (about 6-7 times higher for CNT than for Si). Therefore, a field about 6000 times higher is needed for a Si nanowire with 20 nm diameter compared to a carbon nanotube with 1.4 nm diameter. Consequently, I submit that an impractically high value of conventionally applied electric field (~$4x10^6$ V/cm) is needed for significant deflection (alignment capability) of a 20 nm Si nanowire. For an electric field of

700 V/cm, the achievable deflection for a 20 nm Si nanowire has a negligible value of <1 Å (0.1 nm).

16. I submit that it is not practical to apply such a large field using conventional techniques. On the contrary, one would need a very clever technique (which is outside of the skill set of the ordinarily skilled artisan) that would (1) supply the high field; (2) allow the precursor gas to reach the growing nanowire (quite difficult due to close spacing of the electrodes); (3) not geometrically impede growth; and (4) be compatible with a high temperature, gaseous ambient. The present Declarant is not aware of any technical references having taught or suggested achieving all four of the above requirements. For example, the Kam IEDM paper, *infra*, achieves (1), but not the other requirements.

17. Comparing the teachings of the '017 patent and the Nature Paper, I conclude that one skilled in the art would not be likely to combine such teachings. In fact, I submit that the ordinarily skilled artisan would be led away from combining the teachings of Li with the Nature Paper for the following reasons. Li teaches exposing relatively thin nanowires to an electric field to achieve vertical alignment. The nanowires of the Nature Paper have a relatively thick diameter. If one were to attempt to align the nanowires of the Nature Paper by applying an external electric field as taught by Li, such an electric field would have to be orders of magnitude higher than that taught in Li to vertically align the nanowires. Further, such a field cannot be applied by conventional means. This conclusion may be inferred from an analogous system, wherein an electric field of ~10^7 V/cm (~5 V applied across a 5 nm gap) is also needed to deflect the 25 nm-wide Si field plate of a nanoelectromechanical field-effect transistor (although the situation is slightly different: clamped at both ends, rather than cantilevered from one end). See, for example, H. Kam, et al., 2005 International Electron Devices Meeting, Washington DC, December 5-7, 2005, paper 19.2, a copy of which is attached hereto as Exhibit 2.

18. If one ordinarily skilled in the art were to attempt alignment of the Nature Paper nanowires using the electric fields, plasma techniques and thermal techniques taught by Li, I believe he/she would either fail, or destroy at least one segment of the Nature Paper nanowires for the following reasons.

19. The electric fields used in Li's techniques would not be strong enough to align the Nature Paper nanowires with either an externally applied electric field or in a plasma. In a plasma, the net DC field, as mentioned above, is also only moderate (~KV/cm).

20. I submit that, without undue experimentation, the plasma taught in Li is likely to deleteriously affect at least one of the segments of the nanowires taught in the Nature Paper because, to my knowledge, plasma exposure should be carefully controlled to avoid damaging the materials which are exposed to the plasma. When two or more materials are exposed, the limits of allowable plasma parameters decreases so that it is difficult to provide enough energy to align the nanowire without damaging the more (chemically or mechanically) fragile of the materials in the segmented nanowire. Additionally, if the plasma is used to enable the growth reaction, it is difficult to grow the segment requiring higher energy without damaging the more fragile segment.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and, that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Theodore I. Kamins, PhD. August 25, 2006

Theodore I. Kamins, Ph.D. Date

Electric-field-aligned growth of single-walled carbon nanotubes on surfaces

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(Received 12 August 2002; accepted 13 September 2002)

Aligned single-walled carbon nanotubes are grown onto the surfaces of SiO_2/Si substrates in electric fields established across patterned metal electrodes. Calculations of the electric field distribution under the designed electrode structures, the directing ability of electric fields, and the prevention of surface van der Waals interactions are used to rationalize the aligned growth. The capability of synthesizing oriented single-walled nanotubes on surfaces shall open up many opportunities in organized architectures of nanotubes for molecular electronics. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1518773]

Obtaining organized single-walled carbon nanotube (SWNT) structures is a critical step towards interesting and practical devices of novel molecular wires.[1,2] With two approaches—post-growth assembly and *in situ* controlled growth—progress has been made to reach this goal. In both approaches, electric fields have been exploited to control the orientation of SWNTs,[3,4] utilizing the highly anisotropic polarizability of nanotubes.[5] *In situ* growth by chemical vapor deposition (CVD) in an electric field can direct the orientation of SWNTs, as shown by our group with the nanotubes in suspended form.[3]

While suspended SWNTs with directionality are important to mechanical and electromechanical studies and devices,[6] it is equally important to grow aligned nanotubes resting on surfaces. This ability will then allow successive patterned growth steps in electric fields to produce multiple sets of nanotubes aligned to various directions, and allow metallization and other integration steps to fabricate addressable devices, without the mechanical instability problems of suspended nanotubes. Here, we show that aligned SWNTs on surfaces can indeed be obtained by electric-field-directed CVD growth, with a rational choice of substrates, electrode materials, and structures. The mechanism for alignment involves suitable electric field distributions and the prevention of van der Waals binding with substrate surfaces during nanotube growth.

We started with Si wafers with 1.85-μm-thick thermally grown SiO_2 as substrates. We used molybdenum metal electrodes to establish electric fields on the substrates, as shown in Fig. 1(a). The electrodes were patterned by photolithography and liftoff, each with a dimension of 0.8 cm by 0.3 cm and a thickness of either 50 or 100 nm. The gap between the Mo electrodes was 10 μm. We then patterned a catalyst on top of the two opposing Mo electrodes using a second photolithography step aligned to the electrodes. The catalyst regions on the two electrodes were designed to be 5 μm$\times$0.4 cm strips containing an alumina supported Fe/Mo catalyst,[7] and were $\sim$3–5 μm away from the edges of the Mo electrodes [Fig. 1(b)]. The catalyst patterning step utilized a poly(methylmethacrylate) (PMMA) and photoresist double layer approach. The top photoresist layer was first patterned by standard photolithography. After developing, oxygen plasma was used to etch into and form wells in the PMMA. The top photoresist layer was then fully removed by exposure to a high flux of light and subsequent development. Catalyst material was then deposited from a methanol suspension into the patterned PMMA wells followed by liftoff in acetone.[7] We used the double layer approach so that PMMA can be patterned by standard photolithography and

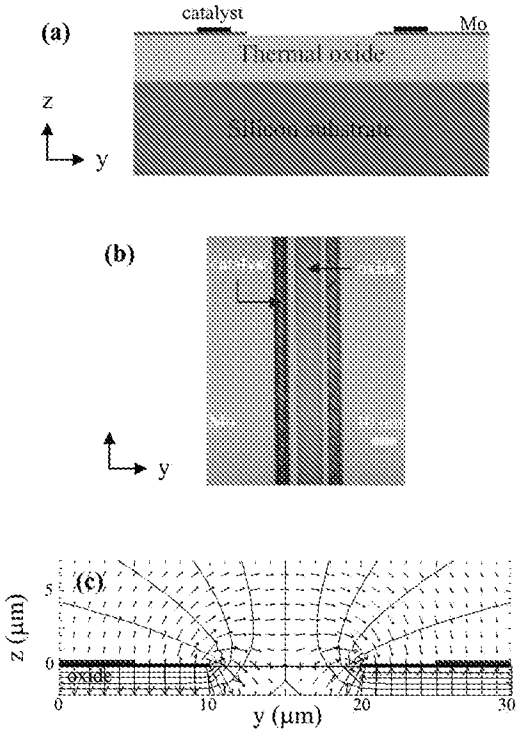

FIG. 1. Structure of samples used for electric field aligned growth of SWNTs on surfaces. (a) Cross-sectional view of the Si/SiO_2 (1.85-μm-thick) substrate, microfabricated Mo electrodes, and the catalyst strips (not to scale). The gap between the Mo electrodes is 10 μm. (b) An optical image showing the top-view of a sample. (c) Electric field distribution and equipotential lines calculated for the left and right Mo electrodes biased at 10 and 0 V, respectively. The underlying Si substrate is floating. The lengths of the field line arrows scale with the strengths of the local fields.

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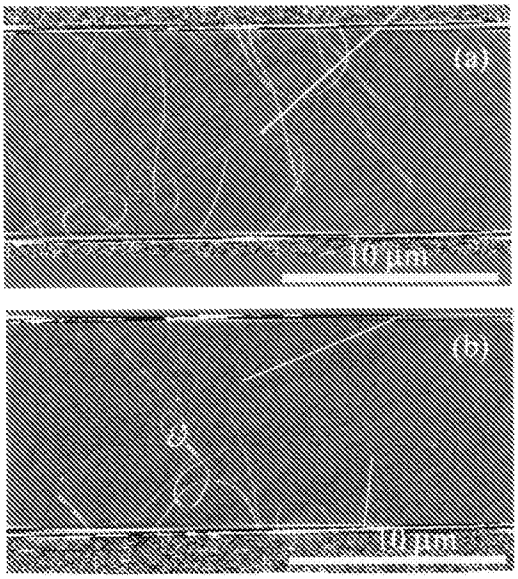

FIG. 2. Random orientations of nanotubes grown by CVD when no electric field is applied in a control experiment. The two AFM images show randomly oriented nanotubes in the gap region between the Mo electrodes. The edges of the Mo electrodes are shown at the top and bottom of each image.

dry etching. The photoresist pattern itself was not used for catalyst patterning due to the incompatibility of photoresist with methanol.

Aligned SWNTs across the gap between the electrodes were grown in a 1 in. CVD system equipped with electrical feedthroughs. The substrate was mounted on a home-made fixture on which two metal stainless steel clips were designed to make electrical contact to the Mo electrodes for applying bias voltages (3–20 V) across the gap. The Si substrate underlying the SiO_2 layer was kept floating. A 40 kΩ serial resistor was used to limit the current. SWNTs were grown at 900 °C for 2 min under 720 mL/min of methane, 500 mL/min of hydrogen, and 12 mL/min of ethylene flow. Pure hydrogen was flown during heating and cooling the CVD system to prevent oxidation of the Mo electrodes by possible oxygen impurities.

The substrates used in the current work were SiO_2/Si wafers (instead of quartz used previously for aligned suspended SWNTs[3]). The 1.85-μm-thick thermally grown SiO_2 layer was found stable against electrical breakdown under 3–20 V applied across the Mo electrodes. Mo was used for electrodes in place of polysilicon, due to its compatibility with high temperature CVD growth conditions without loss of conductivity.[8] These substrate and electrode materials significantly facilitated the current work owing to their simplicity and ease of microfabrication.

Control experiments reveal that, in the absence of electric fields, nanotubes grown from the catalyst regions bridge the electrodes in random orientations, as shown in the atomic force microscopy (AFM) images in Fig. 2. In strong contrast, high degree of alignment is observed for nanotubes grown under applied electric fields between the Mo electrodes. Figure 3 shows AFM data recorded with samples grown by CVD with a 10 V bias voltage applied across the 10 μm gap between the electrodes. The nanotubes are clearly aligned perpendicular to the edges of the electrodes, in the direction of the electric field. Scanning electron microscopy (SEM) imaging has also revealed aligned nanotube structures along the electric field direction (Fig. 4). We have carried out nanotube growth under applied voltages of 3, 5, 10, and 20 V. Alignment appears to be less effective, although still present, when 3 V is applied across the 10 μm gap. On the other hand, no obvious improvement is observed in the alignment of nanotubes when the voltage is increased to 20 V. Further increase in voltage tends to break down the SiO_2 dielectric

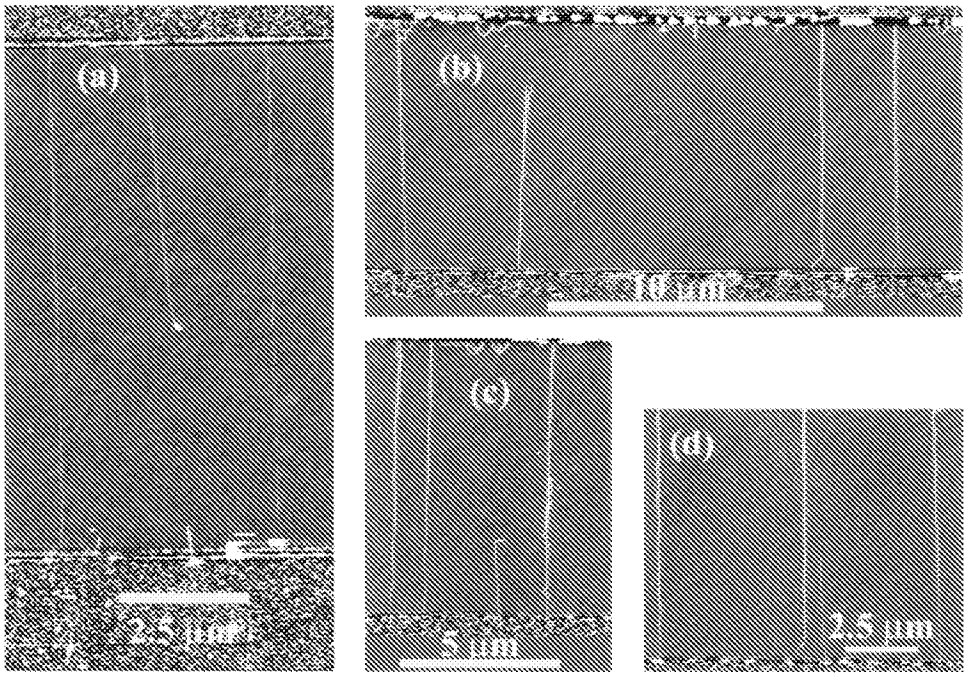

FIG. 3. Aligned nanotubes resting on SiO_2 surfaces after electric field directed growth. The four images were obtained with different samples that had gone through independent electric-field-directed growth runs. The nanotubes show clear alignment in the direction of the electric field, perpendicular to the edges of the Mo electrodes.

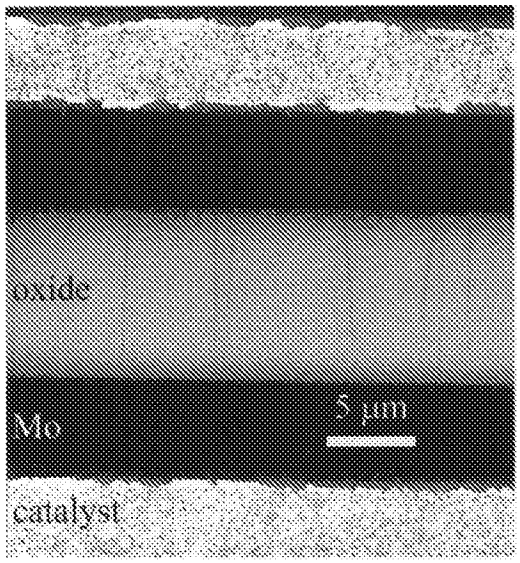

FIG. 4. An SEM image of aligned nanotubes grown by CVD in an electric field. The dark lines in the center region of the image are aligned nanotubes. The nanotubes and the Mo electrodes (regions bridged by the nanotubes) appear dark since they are electrically conducting, whereas the SiO_2 surface in the gap region appears bright due to charging effects under our imaging conditions. The catalyst strips are visible as the top and bottom bright areas.

layer. Thus, we identify that ~10 V applied between the electrodes spaced at 10 μm is optimum for aligned growth of nanotubes on surfaces. Using this condition, we have carried out growth with 20 samples, and observed a reproducible and consistent electric field alignment effect, with only slight variations in the degree of alignment from sample to sample.

To understand the alignment of nanotubes resting on SiO_2 surfaces, we first calculate the electric field distribution for our sample geometry using the MEDICI simulation program (by Avant! Co.) to solve the Laplace equation numerically. Fig. 1(c) shows a cross-section view of electric field vectors and equipotential lines for the sample structure. At the locations of the catalyst strips from which the nanotubes are grown, the electric field is nearly perpendicular to the Mo metal surface, with a field strength of ~0.5 V/μm. Right in the middle of the gap between the two metal electrodes, the electric field is 0.2 V/μm at the SiO_2–air interface. Note that the field lines in the gap are not perfectly parallel to the surface plane in the immediate vicinity of the surface, but are at a small angle. This is caused by the distortion effect of the floating Si substrate underneath the oxide layer.

We suggest that nanotubes grown from the catalyst regions initially extend into the air nearly normal to the metal electrode surface, along the direction of the local electric field. The nanotubes follow the electric field lines as they lengthen, and with the existence of field gradients, they tend to follow the field lines with the highest strength to maximize the interaction between the electric field and the induced dipole moments on the nanotubes.[3] When the nanotubes are over the electrode gap region, they are aligned to the overall field direction in the gap (perpendicular to the electrode edges on the x–y plane), become directed towards the substrate by field gradients, and subsequently fall onto the surface. This results in aligned nanotubes immobilized on the surface by van der Waals forces.

There are two important factors for the aligned growth of SWNTs onto substrates. The first is the directing or aligning ability of the electric field. In our previous work, we have shown that in a field of ~1 V/μm, the induced dipole (~10^6 Debye, largely along the tube axis due to the strong anisotropy in polarizability[5]) on a ~10 μm long SWNT is sufficient to overcome most of the orientation randomizing forces such as thermal vibration.[3] This condition is satisfied here since the electric field strength is on the order of 1 V/μm. An equally important factor is that during growth and lengthening, the nanotubes must stay away from surfaces to avoid capture by the surfaces, so that the nanotubes can fully experience the aligning effect of the electric field. For a nanotube pinned on a surface, strong van der Waals interactions will prevent it from responding to the field directing effect.[3] This condition is also satisfied by our sample design, as the nanotubes grown from the catalyst regions do not contact the substrate until they have been fully aligned to the electric field and guided onto the substrate.

A control experiment was carried out with the same substrate and electrode structures, but different catalyst locations. We placed catalyst, in the form of discrete Fe_2O_3 nanoparticles,[9] onto the SiO_2 surface in the gap region between the two Mo electrodes, and carried out CVD growth under a 10 V applied voltage across the 10 μm gap. The orientations of nanotubes thus grown appear random on the surface without any apparent alignment to the electric field direction inside the gap. We attribute this to the fact that the electric field direction is not normal to the surface at the catalyst sites in the gap region, and that field gradients in this region do not favor nanotubes directing away from the surface. Thus, once reaching a certain length at the early stage of growth, the nanotubes touch the substrate and become pinned.

In summary, we have used *in situ* electric fields to grow aligned SWNTs onto surfaces by CVD. Excellent alignment of nanotubes is obtained on SiO_2/Si surfaces based on a rational choice of materials and sample structure design. These results could lead to the synthesis of complex organized nanotube structures for molecular electronics applications.

This work was funded by the DARPA Moletronics Program and the MARCO MSD Focus Center.

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A New Nano-Electro-Mechanical Field Effect Transistor (NEMFET) Design for Low-Power Electronics

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Abstract

An accumulation-mode design for nanometer-scale electromechanical-gate field effect transistors (NEMFETs) is proposed and studied via simulation. In the off state, the gate electrode is in contact with the thin gate dielectric and short-channel effects are effectively suppressed. In the on state, the gate electrode is separated from the thin gate dielectric so that the threshold voltage V_T is dynamically lowered and the transistor drive current I_{on} is enhanced, and gate leakage is eliminated. The NEMFET can likely meet performance specifications for low-power applications at 25 nm gate length, and is attractive for scaled supply voltage operation.

Introduction

A major challenge for CMOS technology scaling is the limited scalability of the MOSFET threshold voltage (V_T) due to the fundamental thermal (k_BT/q) limit that determines the steepest transition (60 mV/dec at 300K) between on and off states. Alternative transistor designs based on band-to-band tunneling [1] and avalanche junction breakdown [2] have been proposed to overcome this limit. However, sub-60 mV/dec subthreshold swing (S) has yet to be demonstrated in a tunneling FET (TFET), and an avalanche-amplification (IMOS) device requires a non-zero drain-to-source voltage to sustain the breakdown current, which limits its application. In this paper, we present a new nanoscale-electro-mechanical-gate field effect transistor (NEMFET) design which utilizes the ultra-abrupt movement of a mechanical beam (the gate electrode) to achieve $S < 60$ mV/dec and thus enhance the transistor on/off current ratio.

Device Structure and Operating Principle

Previously reported suspended-gate FETs [3] utilized an enhancement-mode design, which requires a high gate voltage ($>V_T$) for pull-in to occur and suffers from severe short-channel effects due to weak gate-to-channel coupling in the off state. In contrast, the NEMFET in this work utilizes an accumulation-mode design to achieve improved performance characteristics. Figs. 1 and 2 show schematic cross-sections of the NEMFET in the off state and on state, respectively. The gate electrode is assumed to be anchored on either side of the channel (in/out of the plane of the figures), thus forming a clamped-clamped beam (with a characteristic spring constant k) suspended over the channel. To suppress stiction between the gate and the channel upon contact [4], the NEMFET must be vacuum-encapsulated [5].

In the off state (gate voltage $V_g = 0$ V), the gate electrode is pulled down (so that it contacts the thin gate dielectric) due to the work-function difference (Φ_{MS}) between the gate and the channel which results in an attractive electrostatic force. The channel region is therefore fully depleted in the off state (Fig. 3). Capacitive coupling between the gate and the channel is therefore maximized to suppress short-channel effects, and the device is in a high-V_T state.

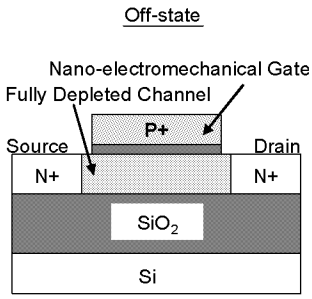

Fig 1. In the off state, the gate is in contact with the thin gate dielectric and the channel is fully depleted, due to the gate-channel work function difference.

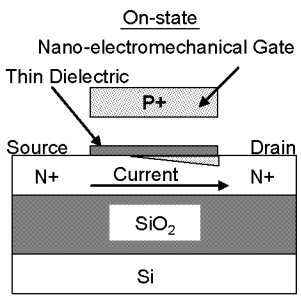

Fig 2. In the on state, the gate is separated from the gate dielectric due to the spring restoring force

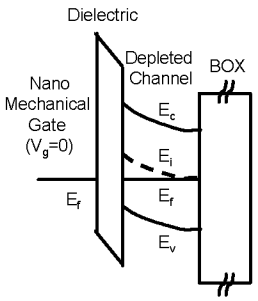

Fig 3. Energy-band diagram for the NEMFET in the off state. Note that the channel is fully depleted.

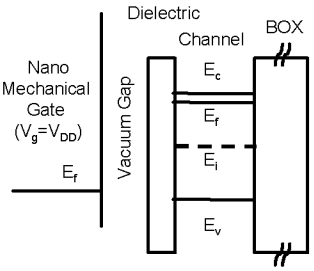

Fig 4. Energy-band diagram for the NEMFET in the on state. Note that the channel is fully conductive.

As V_g is increased, the depletion depth in the channel decreases and hence an increasing amount of current can flow between the source and drain regions. V_g also serves to counteract Φ_{MS}, to reduce the attractive electrostatic force between the gate and the channel. At a critical release voltage V_{on} (for which the electrostatic force equals the spring restoring force of the gate), the gate will abruptly pull away from the channel. As a result, the depletion depth decreases and channel current increases abruptly at $V_g = V_{on}$, and the device enters a low-V_T state. Note that the NEMFET mechanically amplifies the modulation of the channel potential by V_g to achieve $S < 60$ mV/dec, in contrast to the TFET and IMOS devices which amplify charge injection. For sufficiently high V_g, the depletion depth is zero; *i.e.*, the

vertical potential drop (V_g - Φ_{MS}) appears entirely across the gap, and the channel film is fully conducting (Fig. 4). A key feature of the NEMFET is that the gate leakage current is zero in the on state, because the gate electrode is physically separated from the channel by a vacuum gap.

NEMFET Modeling

A self-consistent solution for the gap thickness (x) and channel surface potential $\Phi_{s,front}$ can be found by solving the spring-force equation at physical equilibrium and the electrostatic potential equations for the silicon-on-insulator channel layer (Fig. 5) simultaneously and iteratively, for each combination of gate bias V_g and drain bias V_{ds}. (The source is assumed to be grounded.) Note that the average channel potential (V_{ds}/2) is considered in the electromechanical model. The data sets (V_g, V_{ds}, x) obtained in this manner were then used, along with the physical device parameters shown in Fig. 6, as input parameters for the ISE device simulator [6] to obtain the potential distribution and drain current for the NEMFET for each data set. This first-order model does not incorporate the van der Waals force between the gate and the channel, since it is highly dependent on the topography of the contacting surfaces [7]. Structuring the contacting surfaces may be necessary to minimize the effect of this additional attractive force.

As shown in Fig. 6, the heavily doped source/drain (S/D) regions are laterally offset from the gate electrode. The offset distance (8.5nm) was chosen to optimize the trade-off between low off-state current and high on-state current. Slight misalignment of the electrode gate to the S/D regions should have negligible impact on transistor performance for the accumulation-mode design.

DC Performance Analysis

Solution of the equations in Fig. 5 yields x as a function of V_g, shown in Fig. 7. It can be seen that x increases abruptly at a critical release voltage (V_{on}) as V_g is increased from 0 V, and that x decreases abruptly at a critical pull-down voltage (V_{off}) as V_g is decreased from a high voltage (1 V). V_{on} and V_{off} are not equal, resulting in hysteresis, because of the quadratic nature of the electrostatic force (ref. Equation (1) in Fig. 5). Qualitatively, the electrostatic force required to hold the gate down is less than that required to pull it down, because of the smaller gap thickness in the pulled-down state. V_{ds} reduces the average applied bias between the gate and the channel, resulting in a stronger attractive electrostatic force; thus V_{on} and V_{off} each increase with V_{ds}. Note that for the range of V_g and V_{ds} values considered here, x is less than or equal to 1 nm, which is the gap thickness as fabricated (t_{gap}).

As shown in Fig. 8, the abrupt movement of the gate results in a correspondingly abrupt change in the channel potential profile at $V_g = V_{on}$. This can be equivalently described as a dynamic reduction in V_T as V_g increases to be higher than V_{on}. If V_T for an accumulation-mode MOSFET is defined as the value of V_g for which the channel is just fully depleted, then the change in V_T due to the movement of the gate is approximately $\Delta V_T = -qN_B T_{Si} x/\varepsilon_o$ =0.36V, where N_B is the channel/body doping concentration, T_{Si} is the channel film thickness, and ε_o is the vacuum permittivity.

Figs. 9 and 10 show the simulated NEMFET I_d-V_g and I_d-V_d characteristics, respectively. As compared to a fixed-gate accumulation-mode FET with the same on-state current I_{on}, the NEMFET provides more than $10^5\times$ reduction in I_{off}. As compared to a fixed-gate accumulation-mode FET with the

Mechanics: $F_{net} = \varepsilon_o V_{gap}^2 A/(2x^2) - k(t_{gap} - x) = 0$ - (1)

$V_{gap} = V_{FG} - \Phi_{MS,front} - V_{ox} - \Phi_{s,front}$, where V_{gap}= voltage drop across the vacuum gap, k = spring constant of the mechanical gate, t_{gap}= fabricated gap thickness, V_{ox}= voltage drop across the front gate oxide

Electrostatics: $V_{FG} = V_g = \Phi_{MS,front} + (1 + C_{si}/C_{ox,front})\Phi_{s,front} - (C_{si}/C_{ox,front})(\Phi_{s,back} - V_{ds}/2) - Q_{s,front}/C_{ox,front}$

$V_{BG} = 0 = \Phi_{MS,back} + (1 + C_{si}/C_{ox,back})(\Phi_{s,back} - V_{ds}/2) - (C_{si}/C_{ox,back})\Phi_{s,front} - Q_{s,back}/C_{ox,back}$

$$Q_{s,front} = \sqrt{2\varepsilon_{si}k_BT\left(\frac{n_i^2}{n_o}\left(e^{q\Phi_{s,front}/(k_BT)} + q\Phi_{s,front}/(k_BT) - 1\right) + n_o\left(e^{q\Phi_{s,front}/(k_BT)} - q\Phi_{s,front}/(k_BT) - 1\right)\right)}$$

$$Q_{s,back} = \sqrt{2\varepsilon_{si}k_BT\times\left(\frac{n_i^2}{n_o}\left(e^{q(\Phi_{s,back} - V_{ds}/2)/(k_BT)} + q(\Phi_{s,back} - V_{ds}/2)/(k_BT) - 1\right) + n_o\left(e^{q(\Phi_{s,back} - V_{ds}/2)/(k_BT)} - q(\Phi_{s,back} - V_{ds}/2)/(k_BT) - 1\right)\right)}$$

$$C_{ox,front} = \frac{\varepsilon_o}{(t_{ox}/(\varepsilon_{SiO_2}/\varepsilon_o) + x)} \quad C_{ox,back} = \frac{\varepsilon_{SiO_2}}{T_{BOX}}, \quad C_{si} = \frac{\varepsilon_{Si}}{T_{si}}.$$

Fig 5. Equilibrium equations for NEMFET mechanics and electrostatics, which are solved simultaneously to obtain the equilibrium gap x.

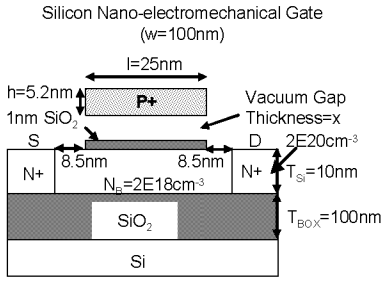

Fig 6. Cross-section of transistor structure used in device simulations. Default values for channel doping (N_B) and thickness (T_{Si}) are indicated.

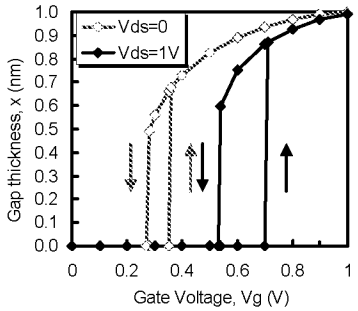

Fig 7. Dependence of gap thickness x on gate and drain voltages. For V_{ds} = 0V, V_{on} = 0.27V and V_{off} = 0.35V. V_{on} and V_{off} shift to 0.53V and 0.7V, respectively, for V_{ds} = 1V. V_{on} and V_{off} also depend on gate dimensions.

same off-state current I_{off}, the NEMFET provides 30% improvement in on-state current I_{on}. Due to the dependence of V_{on} and V_{off} on V_{ds}, negative differential resistance (NDR), with hysteresis is seen in the I_d-V_d characteristics, for moderate values of V_g. This NDR behavior can potentially be exploited for compact circuit design [8].

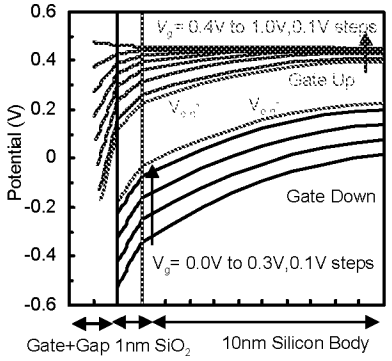

Fig 8. Potential distribution through the gate dielectric and channel, for increasing values of V_g (V_{ds} = 0V). When the gate is released at $V_g = V_{on}$, the channel potential profile changes abruptly.

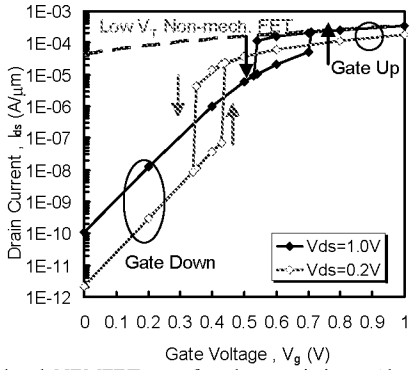

Fig. 9. Simulated NEMFET transfer characteristics. Abrupt changes in current are seen at V_{on} and V_{off} (ref. Fig. 7). I_{on} and I_{off} are 336μA/μm and 110pA/μm, respectively, for V_{ds} = 1V.

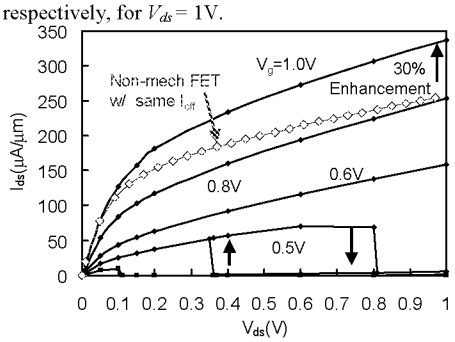

Fig. 10. Simulated NEMFET output characteristics.

Design Optimization

V_{on} and V_{off} must each lie within the subthreshold operation range of V_g in order for the NEMFET to be a dynamic-V_T device. Figs. 11 and 12 show the dependences of V_{on} and V_{off} on N_B and t_{gap}, respectively. The optimal value of N_B lies in the low-10^{18} cm^{-3} range. Note that t_{gap} cannot be much greater than 1 nm; otherwise the gate will not be pulled-down in the off state (at V_g = 0 V). V_{on} and V_{off} will also vary linearly with the gate work function, as does V_T.

Fig. 13 shows how I_{on} and I_{off} change with N_B, for two different values of T_{Si}. N_B must be tightly controlled to minimize performance variation, as is generally the case for accumulation-mode FET designs. Thinner T_{Si} can yield better I_{on}/I_{off}, but at higher N_B which increases V_{on} and V_{off}. With modest enhancement in I_{on} achieved by process-induced strain, the NEMFET can be expected to meet industry performance targets for 25 nm gate length [9].

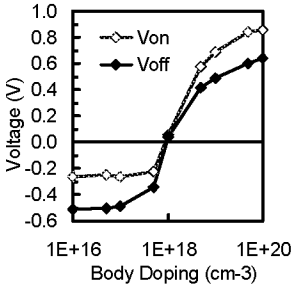

Fig. 11. Dependence of V_{on} and V_{off} on channel/body doping. An increase in N_B increases the work function difference Φ_{MS} and thus a larger gate voltage is needed to release/pull-down the gate electrode.

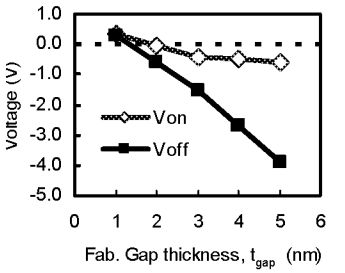

Fig. 12. Dependence of V_{on} and V_{off} on the fabricated gap thickness t_{gap}. A larger initial gap means a larger spring restoring force. Thus, the gate electrode is released/pulled-down at a lower gate voltage.

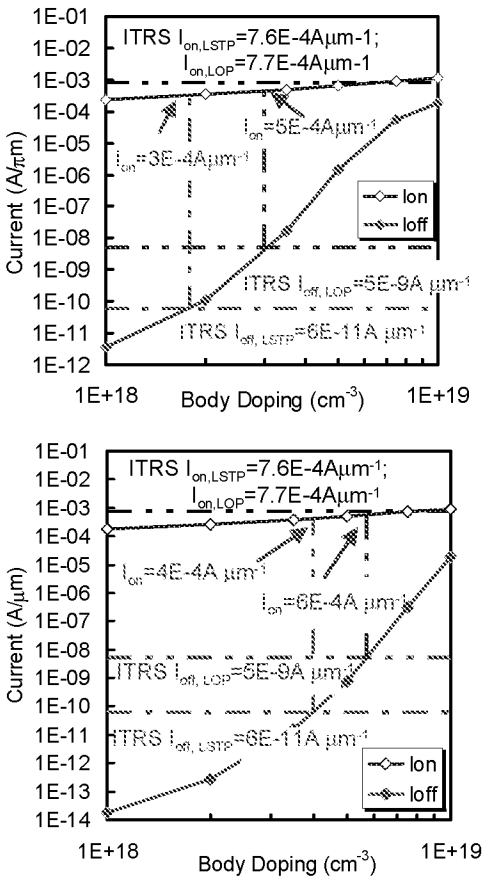

Fig. 13. I_{on} and I_{off} *vs.* channel/body doping for T_{si} = 10nm (top) and T_{Si} = 8nm (bottom). ITRS targets for low operating power (LOP) and low standby power (LSTP) applications are indicated [9].

AC Performance Analysis

As the effective gate oxide thickness (EOT) changes with the gate voltage, the average gate capacitance of the NEMFET is found by integration:

$$\int_0^{V_{dd}} C_g(V_g)dV_g/V_g \Big|_{V_{ds}=1V} = 0.66\text{fF}/\mu\text{m}$$

The spring constant of the gate (k), which is a doubly clamped beam, can be estimated as:

$$k = \frac{16Elh^3}{w^3} = 9.5\mu N/\mu m$$

where E=170GPa is the Young's Modulus of silicon

The dynamic power dissipation of the NEMFET consists of two main parts: the electrical charging/discharging of capacitances ($P_{Electrical}$) and the mechanical deformation of the gate ($P_{Mechanical}$):

$$P_{Electrical} = C_g W V_{DD}^2 f_{0->1}; \quad P_{Mechanical} = \tfrac{1}{2} k x^2 f_{0->1}$$

Assuming $f_{0->1}$=1GHz: $P_{Electrical}$= 66 nW and $P_{Mechanical}$= 4.75 nW. The mechanical deformation power is thus expected to be a small portion of the total dynamic power dissipation (in the above case = 6.8%), due to the tiny displacement (1 nm) of the mechanical gate.

The switching speed of the NEMFET can be limited by two factors: the speed of the gate movement (inverse resonant frequency $(\sqrt{k/m})^{-1}$, where m is the mass of the mechanical gate) and the intrinsic delay (C_gV_{DD}/I_{on}). Under constant ratio scaling, the mass decreases more rapidly than the spring constant of the mechanical gate. So, in the nanoscale regime, the gate resonant frequency can be in the GHz range. For example, the resonant frequency of the gate is 18 GHz for the design (Fig. 6) studied in this work. The intrinsic delay is ~2 ps, however, so that the switching speed of the NEMFET is dictated by the mechanical delay. This will limit its application to <10 GHz operating frequencies.

NEMFET with Scaled Supply Voltage

To leverage fully the benefit of a sub-k_BT/q transistor for low-power electronics, the supply voltage (V_{DD}) should be aggressively scaled down in order to lower dynamic power consumption. Figs. 14 and 15 show the simulated I_d-V_g and I_d-V_d characteristics, respectively, for a NEMFET utilizing a 5.3-nm-thick gate electrode with 5.05 eV work function (*e.g.* heavily p-type doped silicon-germanium alloy [10]) which provides for lower V_{on} and V_{off}. For a supply voltage of 0.5 V, I_{on} and I_{off} are 104 μA/μm and 124 pA/μm, respectively. As compared to fixed-gate accumulation-mode FET designs, these represent a 13× improvement in I_{on} or 10^5 reduction in I_{off}.

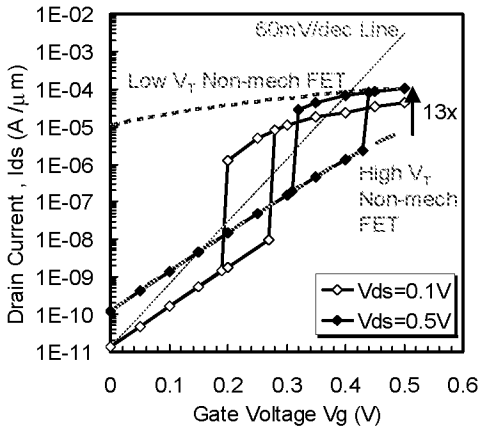

Fig. 14. Simulated NEMFET transfer characteristics for V_{DD} = 0.5V. For reference, a line with 60mV/dec slope is shown. Also, the curves for a fixed-gate, high-V_T FET (with same I_{off} as for the NEMFET) and for a fixed-gate, low-V_T FET (with same I_{on} as for the NEMFET) are shown for reference.

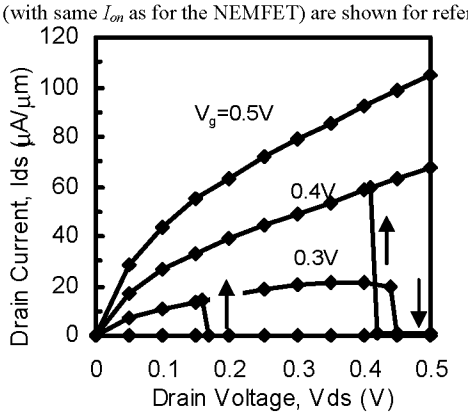

Fig. 15. Simulated NEMFET I_{ds}-V_{ds} output characteristics.

Conclusion

A new accumulation-mode NEMFET device is proposed and is shown to be capable of sub-60 mV/dec switching. Its dynamic-V_T characteristic is advantageous for improving I_{on}/I_{off} and facilitating V_{DD} scaling, and its gate leakage current is zero in the on state. These features make the NEMFET an attractive candidate for low-power electronics applications.

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